

	Type	L #	Hits	Search Text	DBs	Time Stamp
<b>1</b>	BRS	L1	560727	controller or (control adj processor)	US- PGPUB; USPAT	2005/10/25 14:32
<b>2</b>	BRS	L2	2634	fast adj2 clock	US- PGPUB; USPAT	2005/10/25 14:33
<b>3</b>	BRS	L3	4212	(high adj speed) adj2 clock	US- PGPUB; USPAT	2005/10/25 14:34
<b>4</b>	BRS	L4	6551	2 or 3	US- PGPUB; USPAT	2005/10/25 14:34
<b>5</b>	BRS	L5	1906	slow adj2 clock	US- PGPUB; USPAT	2005/10/25 14:34
<b>6</b>	BRS	L6	781	(low adj speed) adj2 clock	US- PGPUB; USPAT	2005/10/25 14:35
<b>7</b>	BRS	L7	2582	5 or 6	US- PGPUB; USPAT	2005/10/25 14:35
<b>8</b>	BRS	L8	627	1 and 4 and 7	US- PGPUB; USPAT	2005/10/25 14:36
<b>9</b>	BRS	L9	645305	input\$4 near3 (signal data)	US- PGPUB; USPAT	2005/10/25 14:37
<b>10</b>	BRS	L10	738438	output\$4 near3 (signal data)	US- PGPUB; USPAT	2005/10/25 14:37
<b>11</b>	BRS	L11	508	8 and 9 and 10	US- PGPUB; USPAT	2005/10/25 14:41
<b>12</b>	BRS	L12	39389	(standard system) adj2 clock	US- PGPUB; USPAT	2005/10/25 14:41
<b>13</b>	BRS	L13	603	multiply\$3 same (5 or 6 or 12)	US- PGPUB; USPAT	2005/10/25 14:42
<b>14</b>	BRS	L14	15	11 and 13	US- PGPUB; USPAT	2005/10/25 15:39
<b>15</b>	BRS	L15	11477	(clock near5 cycle\$1) same (configur\$4 program\$5)	US- PGPUB; USPAT	2005/10/25 15:42

	Type	L #	Hits	Search Text	DBs	Time Stamp
<b>16</b>	BRS	L16	113	11 and 15	US- PGPUB; USPAT	2005/10/25 15:41
<b>17</b>	BRS	L17	2533	(clock near5 cycle\$1) near5 (configur\$4 program\$5)	US- PGPUB; USPAT	2005/10/25 15:42
<b>18</b>	BRS	L18	46	11 and 17	US- PGPUB; USPAT	2005/10/25 15:42
<b>19</b>	BRS	L19	2591	713/400-501.ccls.	US- PGPUB; USPAT	2005/10/25 15:43
<b>20</b>	BRS	L20	1186	713/503.ccls. 713/600.ccls.	US- PGPUB; USPAT	2005/10/25 15:43
<b>21</b>	BRS	L21	3246	19 or 20	US- PGPUB; USPAT	2005/10/25 15:44
<b>22</b>	BRS	L22	10	18 and 21	US- PGPUB; USPAT	2005/10/25 16:16
<b>23</b>	BRS	L23	67	16 not 18	US- PGPUB; USPAT	2005/10/25 16:16
<b>24</b>	BRS	L24	14	23 and 21	US- PGPUB; USPAT	2005/10/25 16:16

	Type	L #	Hits	Search Text	DBs	Time Stamp
<b>1</b>	BRS	L1	3972	(control adj processor).clm.	US- PGPUB; USPAT	2005/10/25 18:41
<b>2</b>	BRS	L2	171942	controller.clm.	US- PGPUB; USPAT	2005/10/25 18:41
<b>3</b>	BRS	L3	175004	1 or 2	US- PGPUB; USPAT	2005/10/25 18:41
<b>4</b>	BRS	L4	161	(fast adj clock).clm.	US- PGPUB; USPAT	2005/10/25 18:42
<b>5</b>	BRS	L5	238	(high adj speed adj clock).clm.	US- PGPUB; USPAT	2005/10/25 18:42
<b>6</b>	BRS	L6	395	4 or 5	US- PGPUB; USPAT	2005/10/25 18:43
<b>7</b>	BRS	L7	32479	(standard system slow) adj clock	US- PGPUB; USPAT	2005/10/25 18:43
<b>8</b>	BRS	L8	3809	7.clm.	US- PGPUB; USPAT	2005/10/25 18:45
<b>9</b>	BRS	L9	5809	(multipl\$4 near5 clock).clm.	US- PGPUB; USPAT	2005/10/25 18:46
<b>10</b>	BRS	L10	467	8 and 9	US- PGPUB; USPAT	2005/10/25 18:47
<b>11</b>	BRS	L11	478806	input.clm.	US- PGPUB; USPAT	2005/10/25 18:47
<b>12</b>	BRS	L12	598880	output.clm.	US- PGPUB; USPAT	2005/10/25 18:47
<b>13</b>	BRS	L13	10487	(clock near5 cycle\$1).clm.	US- PGPUB; USPAT	2005/10/25 18:48
<b>14</b>	BRS	L14	2	3 and 6 and 8 and 10 and 11 and 12 and 13	US- PGPUB; USPAT	2005/10/25 18:49